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Design a Novel Neutral Point Clamped Inverter Without AC booster for Photo-voltaic System

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***Abstract*— *AC booster photovoltaic (PV) inverters are increasingly favored in grid-connected solar installations for their compact structure and enhanced efficiency. However, conventional AC booster designs often face issues with fluctuating common-mode voltage (CMV), which contributes to elevated common-mode leakage current (CM-LC) due to the absence of galvanic isolation. These challenges can negatively impact overall system performance, safety, and conformity to grid regulations. In response to these concerns, this work presents a novel Neutral Point Clamped (NPC) inverter configuration named the H6-Diode (H6-D) topology. This approach combines the low-loss switching capability of AC bypass techniques with a mechanism to effectively suppress CM-LC. A key feature of the topology is a clamping circuit that limits the freewheeling voltage to half of the DC-link level, thereby reducing leakage currents significantly. The design's validity is confirmed through detailed simulations conducted in MATLAB/Simulink and supported by experimental trials using a developed laboratory prototype.*

Keywords*— AC booster, Common mode voltage, Leakage current, Non-NPC, NPC inverter, Total harmonic distortion, Efficiency.

I. INTRODUCTION

Photovoltaic (PV) energy is increasingly recognized for its environmental benefits and its expanding role in sustainable energy solutions[1-3]. In grid-connected PV systems, inverters play a pivotal role in converting DC power to AC and are typically categorized based on the presence or absence of transformers. Traditional inverters with transformers often face challenges such as bulkiness, increased weight, higher costs, and notable power losses. To address these issues, AC booster PV inverters which operate without transformers have been developed and are garnering significant attention across various sectors.However, the absence of galvanic isolation in AC booster inverters introduces technical challenges [3-6]. Notably, it can lead to fluctuating common-mode voltages (CMV), resulting in elevated common-mode leakage currents (CM-LC). These leakage currents can adversely affect system performance, compromise safety, and causeelectromagnetic interference (EMI) issues. According to the VDE-AR-N 4105 standard, if the leakage current exceeds 300 mA, the PV system must disconnect from the grid to ensure safety[6-10].To mitigate CM-LC, various strategies have been proposed, primarily focusing on two approaches [10-15]:

1. **Non-Neutral Point Clamped Methods (non-NPCM):** This approach involves creating a freewheeling current path that separates the grid from the PV arrays, thereby reducing CM-LC.
2. **Incorporation of Additional Clamping Branches:** By adding clamping circuits, this

method aims to stabilize the CMV and suppress leakage currents effectively.

These solutions are crucial for enhancing the reliability and safety of distributed PV systems, ensuring compliance with grid standards, and promoting the broader adoption of AC booster inverters in renewable energy applications.

II. PROPOSED METHODOLOGY

To sustain a consistent common-mode voltage (CMV) and minimize common-mode leakage current (CM-LC), the neutral-point-clamped method (NPCM) is frequently employed in inverter designs. Recent advancements have seen the adoption of super-junction metal-oxide-semiconductor field-effect transistors (SJ-MOSFETs) as power devices to enhance the efficiency of photovoltaic (PV) systems. However, SJ-MOSFETs are prone to significant reverse recovery issues, potentially leading to shoot-through effects between complementary switches, thereby complicating the design of AC booster photovoltaic inverters. To address these challenges, various inverter topologies utilizing MOSFETs as primary power devices have been developed to achieve optimal European (EU) efficiency. For instance, SMA introduced a non-NPC H5 topology by adding an additional switch between the DC side of the PV panel and the H4 circuit legs. Similarly, Sunway proposed the "Highly Efficient and Reliable Inverter Concept" (HERIC) for high-efficiency applications, incorporating a freewheeling branch with two IGBTs and four MOSFETs to enhance EU efficiency. However, non-NPC topologies like H5 and HERIC exhibit suboptimal common-mode behavior throughout the grid cycle. In conclusion, while AC booster PV inverters offer a promising solution for efficient and eco-friendly energy conversion in PV systems, addressing CM-LC issues and optimizing inverter designs remain critical areas for ongoing research and development.

Conversely, topologies utilizing the Neutral-Point-Clamped Method (NPCM) provide both galvanic separation and efficient clamping of common-mode (CM) voltage [16–18]. One example is the HBZVR configuration, which adopts a rectifier bridge circuit consisting of a single active switch (S5) and four diodes (D1–D4) located at the midpoint of the DC-link capacitor, as depicted in Fig. 1(b) [13]. Despite its structural simplicity, this topology fails to maintain consistent CM voltage during freewheeling intervals due to insufficient clamping. To mitigate this limitation, the HBZVR-D variant incorporates an extra diode, ensuring consistent CMV and minimizing leakage currents throughout the entire grid cycle, as shown in Fig. 1(c) [14]. Iteration, termed HB-ZVSCR, was later introduced to further improve CM behavior, as illustrated in Fig. 1(d) [15].

Additionally, Positive-Negative NPC (PN-NPC) and H6-family AC booster inverter structures have emerged, integrating bidirectional active clamping networks, shown in Fig. 1(e) and (f) [16–20]. These designs clamp the CMV to half of the input DC voltage, which significantly reduces CM-LC. However, this benefit comes at the cost of higher energy losses, especially during freewheeling operation, due to the increased number of active switching elements (S2, S5, S7, and S8).

While galvanic isolation remains vital for safety and performance, it alone does not entirely resolve CM-LC challenges. Influences from device junction capacitance and stray parasitics remain problematic [18–20]. Therefore, continuous refinement in inverter topology and component selection is imperative. For example, the oH5 configuration employs a CM-active clamping strategy by integrating an additional switch between the DC-link midpoint and inverter arms [17]. This approach aids in stabilizing CMV but fails to sustain it during dead-time intervals. A more refined topology—the H6 structure introduced in [20]—uses two active switches and two passive diodes positioned between the bridge arms and the DC-link center. Although this approach helps regulate CMV more effectively, it still encounters certain operational limitations, such as vulnerability to shoot-through in non-NPC setups.

Moreover, the reliance on IGBT switches in such designs hinders their performance due to higher switching losses and slower dynamic responses compared to MOSFET counterparts, resulting in suboptimal European (EU) efficiency. Enhancements to the Heric topology have led to the development of the Oheric inverter, as detailed in [22–23], which introduces two additional IGBTs (S7, S8) at the midpoint of the DC-link capacitor to strengthen CM control and suppress leakage currents. Still, both H6 and Oheric topologies exhibit increased conduction losses due to the number of active switches involved during the freewheeling phase.

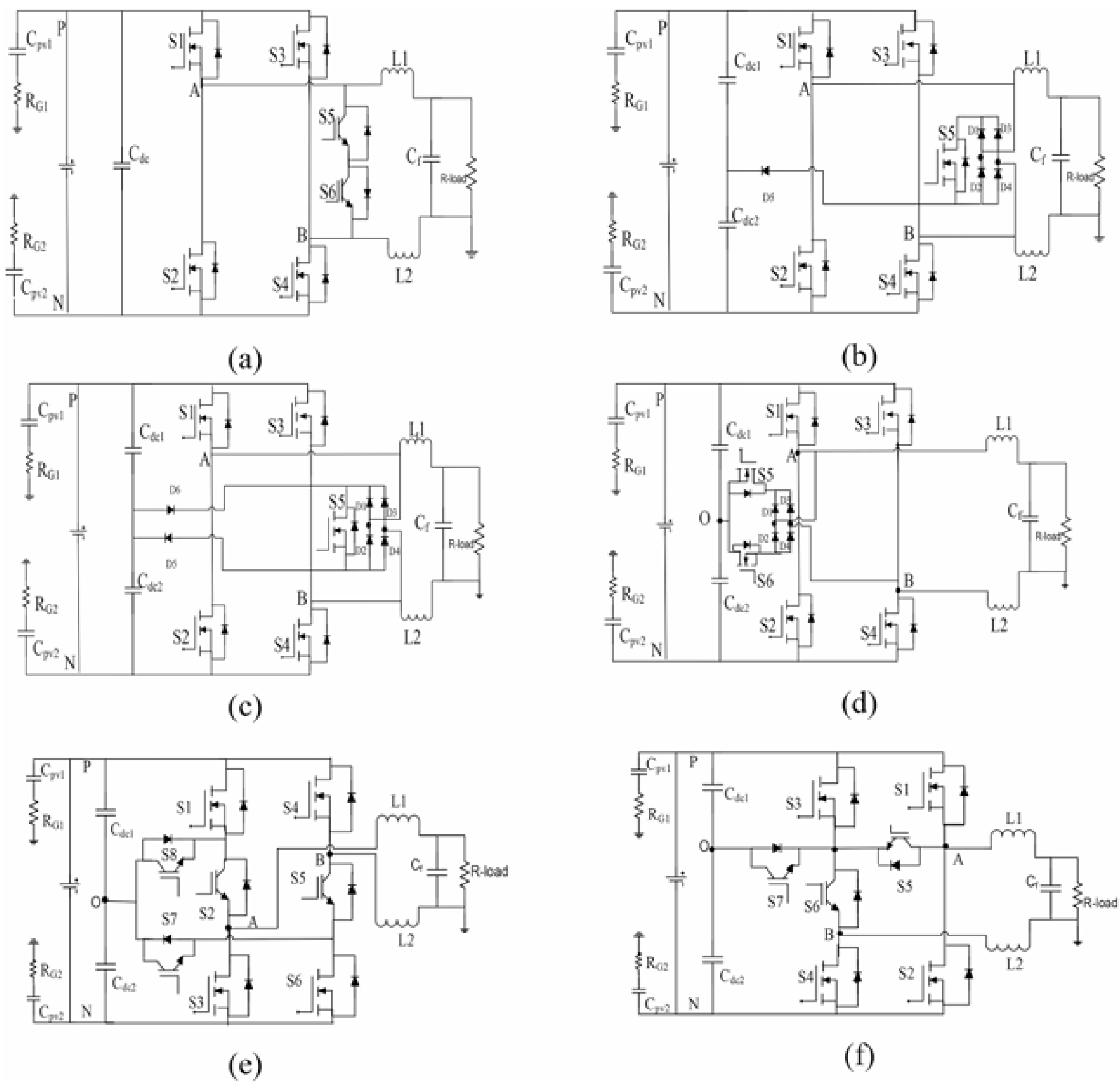

Fig. 1. Existing single-phase TL-PVI topologies: (a) Heric (b) HBZVR, (c) HBZVR-D, (d) HBZVSCR, (e) PN NPC and (f) proposed technique.

Alternative clamped inverter solutions such as the I-NPC and T-NPC types have also been proposed [24–25]. The I-NPC design uses two passive diodes for clamping, while the T-NPC topology utilizes bidirectional switches located at the DC-link midpoint. These designs typically operate at twice the DC input voltage (2Vdc) in full-bridge implementations [26,28,29]. Furthermore, another H6-type inverter using MOSFETs is presented in [27–30], offering refined CMV control and effective CM-LC mitigation. Despite these advantages, it still suffers from high component demands during freewheeling, contributing to greater energy loss.

Building upon the NPCM-based H6 framework, a newly developed H6 MOSFET configuration—termed the H6-D Neutral-Point-Clamped inverter is introduced. This novel topology integrates an AC-bypass strategy with CM-LC suppression through advanced clamping techniques. Key attributes of the H6-D topology include:

- CMV is consistently maintained at 0.5Vdc, effectively driving CM-LC close to zero.
- Shoot-through risks are entirely mitigated.
- Reverse recovery losses are eliminated.
- Total system losses are significantly reduced.
- Switching stress on clamping components is minimized.
- EU efficiency is notably improved.

This H6-D MOSFET inverter represents a holistic solution by merging minimal-loss switching with

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advanced leakage current control. It is particularly well-suited for future AC booster inverter applications in PV systems, where reactive power control during non-unity power factor operation is a key requirement. Comparative analysis between the proposed H6-D and other non-NPC topologies (e.g., Heric, HBZVR) as well as NPC alternatives (e.g., HBZVSCR, PN-NPC, H6-1) is performed using metrics such as CMV, CM leakage, total harmonic distortion (THD), switching stress, loss profile, and overall efficiency. These comparisons are validated through both simulation results and experimental verification.

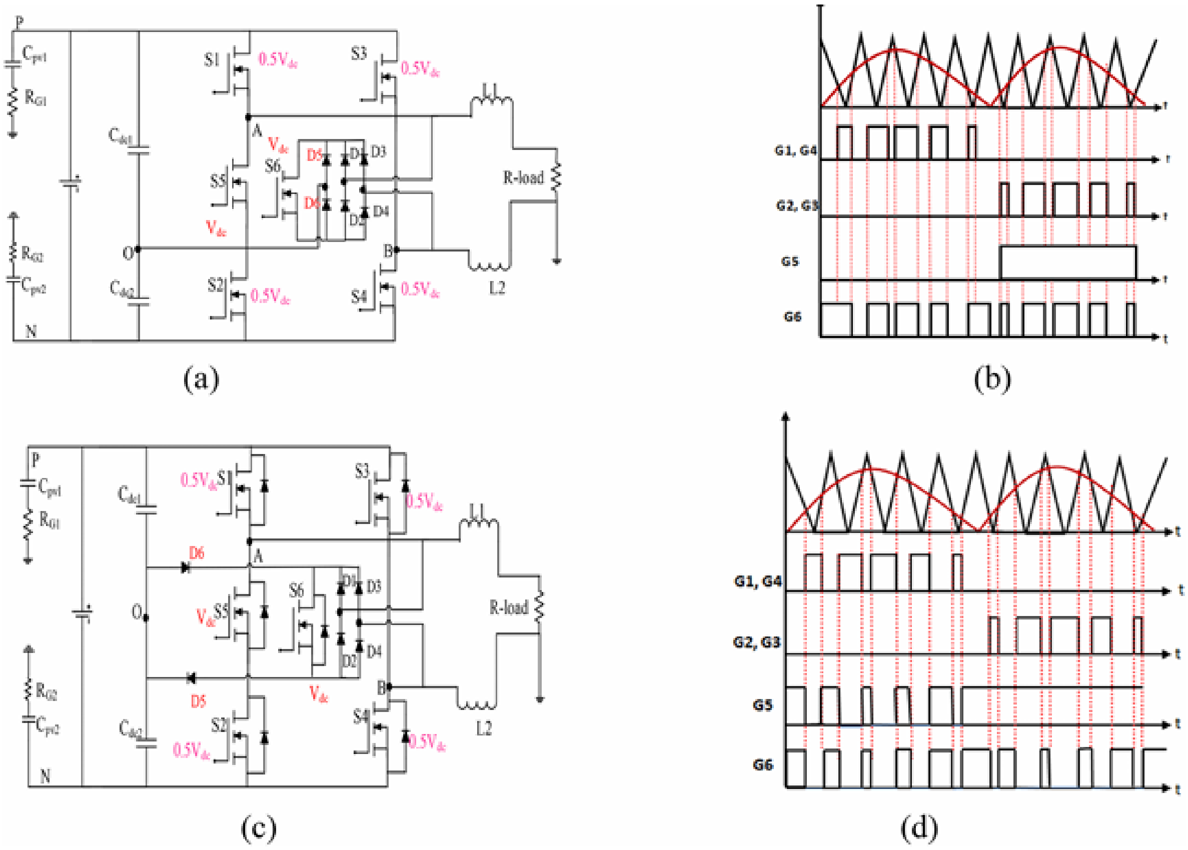

Fig. 2 Proposed new topologies. (a) Circuit Structure (b) unity power factor gate pulses, (c) Variant of H6-D, (d) Non unity power factor gate signals.

III. SIMULATION VALIDATION

The performance of the proposed H6-D topology was rigorously validated through comparative simulation studies involving both non-NPC and NPC configurations. The simulations employed key system parameters, including a DC input voltage of 400 V, parasitic capacitances (CPV1 and CPV2) set at 100 nF, and grounding resistances (RG1 and RG2) of 11 Ω. The setup also utilized two identical filter inductors (L1 and L2) each rated at 3 mH, with a consistent switching frequency of 10 kHz [4]. These conditions established a reliable framework for evaluating the H6-D inverter's performance in terms of common-mode voltage (CMV), common-mode leakage current (CM-LC), total harmonic distortion (THD), switching losses, and overall efficiency.

3.1 Analysis of Output and Common-Mode Behavior

Simulation outputs, illustrated in Figures 3 and 4, depict the voltage and current waveforms (V_{out}, I_{out}, and i_leak) along with the common-mode parameters (V_{AN}, V_4, V_{BN}) for both non-NPCM and NPC-based inverters. Each of the configurations generated a three-level output waveform (+V_{PV}, 0, - V_{PV}) and produced sinusoidal output currents. Nevertheless, the HERIC topology exhibited substandard common-mode behavior, deviating from theoretical expectations due to uncontrolled phase-leg voltages (V_{AN} and V_{BN}). This resulted in a CMV fluctuation near 230 V, as seen in Fig. 4(a), ultimately inducing elevated CM leakage currents as depicted in Fig. 3(b). This instability stems largely from poor clamping control during the freewheeling intervals.

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Consequently, HERIC and other non-NPC topologies fail to effectively suppress CM leakage currents, as shown in Fig. 3(a). A similar issue was observed in the HBZVR topology, which demonstrated the poorest CM characteristics, with noticeable voltage spikes in $V_{\_AN}$ and $V_{\_BN}$. These fluctuations reinforce the understanding that neither galvanic isolation nor standard PWM techniques alone can ensure CMV stability. Hence, HBZVR is also classified under non-NPC designs and displays performance trends comparable to HERIC.

In contrast, NPC-based configurations such as HBZVR-D, HBZVSCR, PN-NPC, and H6-1 exhibited superior CM performance. These topologies maintained steady phase-leg voltages and a stable CMV around 200 V throughout the switching cycle, as illustrated in Figs. 4(c–f). As a result, they successfully suppressed CM leakage currents to near-zero levels, as verified in Figs. 3(c–f). The proposed H6-D inverter further elevates CM control through its advanced clamping branch, which effectively eliminates voltage spikes in V_AN and V_BN due to their complementary switching. As seen in Fig. 4(g), the CMV remains fixed at 200 V, completely nullifying CM-LC, as confirmed in Fig. 3(g).

3.2 Switching Stress and Reverse Recovery Loss Analysis

To verify the stress on switching components and validate the absence of reverse recovery effects in the body diodes, additional waveforms are presented in Fig. 4. details the voltage stress across all six switches within the H6-D design. Four switches (S1 to S4) operate under half of the total DC-link voltage ($0.5V_{\_dc}$), while switches S5 and S6 handle the full $V_{\_dc}$. This voltage-sharing approach reduces the stress across most switches, allowing the use of lower-rated MOSFETs and contributing to reduced conduction losses.

Moreover, Fig. 4(b) displays the body diode currents of the MOSFETs. The absence of negative spikes or transitions confirms that reverse recovery losses are effectively eliminated in the H6-D topology. This leads to lower switching losses and directly enhances the system's operational efficiency and long-term reliability. Thus, the H6-D configuration proves to be a highly efficient and robust solution for low-voltage photovoltaic applications. A comparative overview of performance metrics for various inverter designs is summarized in Table 1.

Table 1. Summary and comparison of discussed topologies among proposed H6-D topology.

Topology	Vout	Iout	VAN	VBN	CMV	CM-LC
HERIC	Unipolar	Sinusoidal	Oscillations (~220V)	Oscillations	Floating (~200V)	< 0.3 A
HBZVR	"	"	"	"	"	< 0.3 A
HBZVR-D	"	"	No Oscillations	"	"	"
PN-NPC	"	"	"	"	"	"
HBZVSCR	"	"	"	"	"	"
H6-I	"	"	"	"	"	"
H6-D	"	"	"	"	"	"

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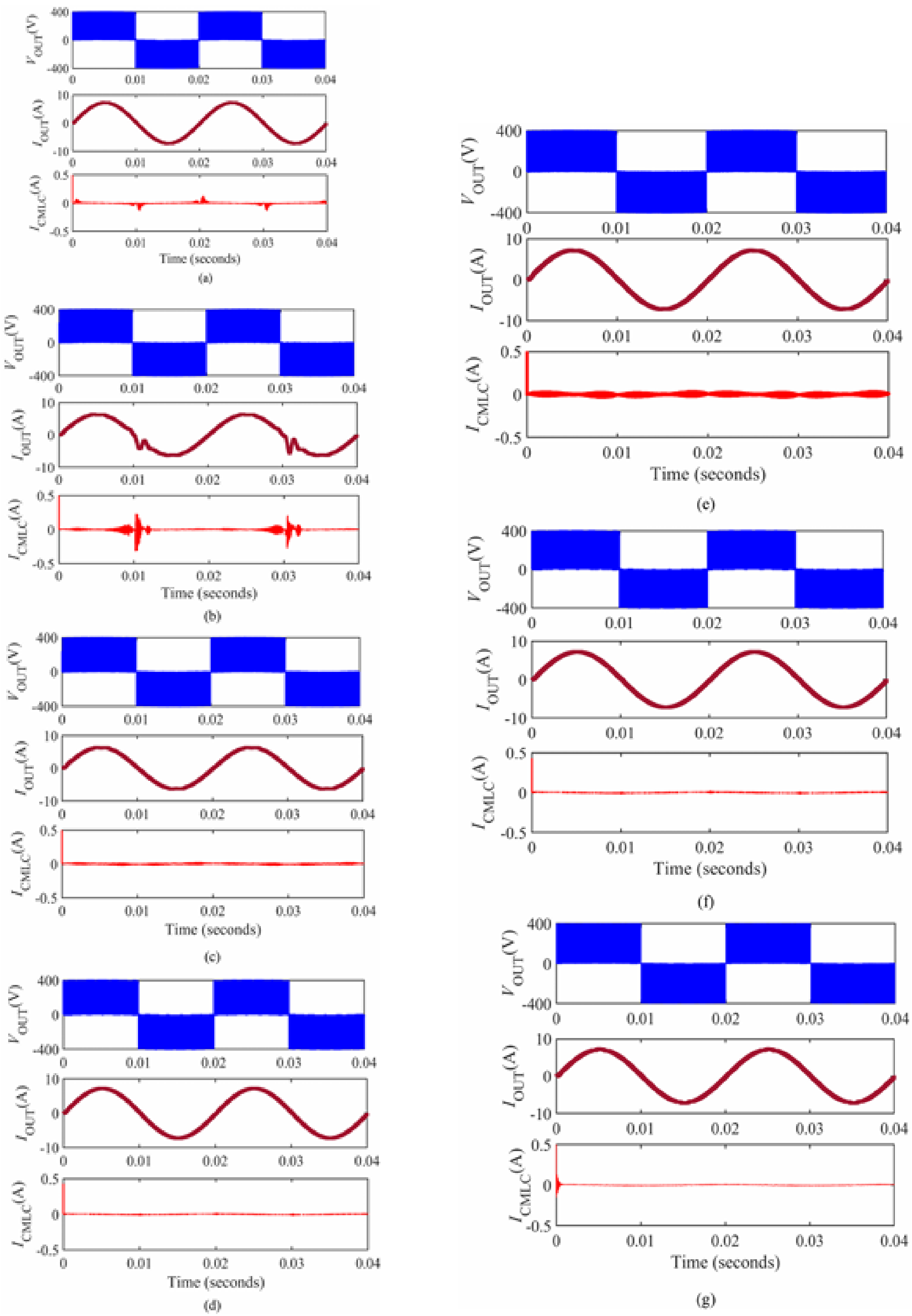

Fig. 3. The Simulation results of Vout (upper), iout (central) and i leak (lower) for (a) HERIC, (b) HBZVR, (c) HBZVR-D, (d) PN-NPC (e) HBZVSCR, (f) H6-I and (g) proposed H6-D TL-PVI topologies

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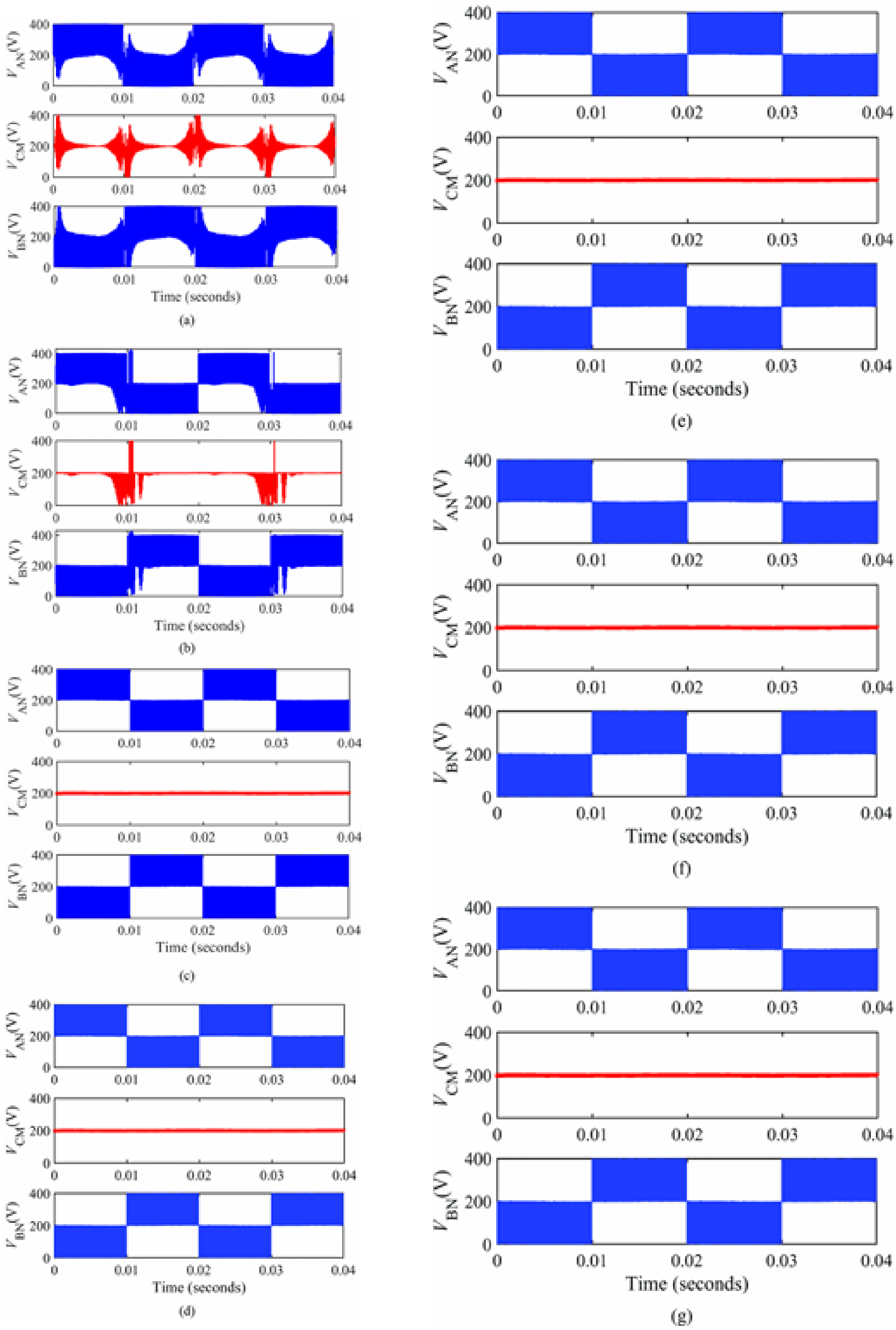

Fig. 4. The Simulation results of V_{AN}, $V_{CM}$and$V_{BN}$for (a) HERIC, (b) HBZVR, (c) HBZVR-D, (d) PN-NPC , (e) HBZVSCR, (f) H6-I and (g) proposed H6-D TL-PVI topologies.

IV. CONCLUSIONS

This table presents a concise comparison of various single-phase V booster photovoltaic (PV) inverter topologies—both non-neutral-point-clamped (non-NPC) and neutral-point-clamped (NPC). It evaluates their efficiency, common-mode (CM) performance, and technical trade-offs, concluding with the proposal of a new H6-D topology that unifies the strengths of both categories (as shown in table 2).

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Table 2. Summary and comparison of discussed topologies among proposed topology.

Topology	Type	Efficiency	CM Performance	CM-LC Reduction	Losses	Remarks
HERIC	Non-NPC	High	Poor (Oscillating CMV)	Low	Low	Efficient but lacks good CM behavior
HBZVR	Non-NPC	High	Poor (Voltage Spikes)	Low	Low	Suffers from high CM leakage despite clamping
HBZVSCR	NPC	Moderate	Excellent (Stable CMV)	High	Moderate–High	Improved CMV stability and CM-LC suppression
PN-NPC	NPC	Moderate	Excellent	High	Higher	Effective CM control but increases conduction complexity
H6-1	NPC	Moderate	Excellent	High	Higher	Great CM performance but suffers from higher device count
(Proposed)	NPC Hybrid	Very High	Excellent (Constant CMV)	Very High	Very Low	Combines low losses and strong CM suppression; optimizes inverter performance

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