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Design a Neutral Point Clamped Multilevel Inverter Over-Modulated Single Reference Double Carrier PWM Technique for the Small Power Solar Panel

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***Abstract*— *In this paper the inverter has been simulated to operate in over-modulation region to utilize maximum of the DC bus voltage. During the operation of NPC in over-modulation zone, the output has flat topped waveform i.e. the upper part gets clipped-off because of operation in over-modulation. By considering, NPC inverter as a system based on single pole triple throw switch so that it can be applied ±0.5V_{dc} and zero voltage at the load terminal is achieved. The number of level counts on the basis of the line-to-line pole voltage so can also be called a 5-level inverter as we have shown, in this paper, the number of levels is equivalent to the number of pole voltages.*

***Keywords*— Neutral-Point Clamped Multilevel Inverter, Total Harmonic Distortion, Voltage Source Inverter, Over-Modulation**

I. INTRODUCTION

As a result, in high-power and medium-voltage situations such as laminators, mills, conveyors, pumps, fans, blowers, compressors, and so on and so., a multilevel power converter structure was introduced as an alternative [1]. As a value-effective solution, multi-level converters not just achieve high power ratings [2] but also allow the use of low-power applications in renewable sources of energy such as photovoltaic, wind, and fuel cells that can be easily networked with a high-power application multi-level converter system.

Power Electronics was officially developed in 1901 because of Peter Cooper Hewitt's innovation of the glass-bulb mercury-arc rectifier [3]. Later, in the 1930s, it moved through the phases of gas tube electronics and the 1940's saturable core magnetic amplifiers. With the invention of the thyristor or silicon controlled rectifier (SCR), the present age of solid-state power electronics has begun. The earliest paper on P-N-P-N activating transistors was published by Bell Laboratories of the United States in 1956 [4], and then GE officially launched the thyristor in 1958. Since then, as shown in Figure 1.2, there has been a massive expansion of technology with research and development exhibiting in various directions. A lot of new devices with higher power levels and better features appeared as a result of the scientific work [5]. When new devices evolved, several new converter topologies were implemented along with advanced Pulse Width modulation (PWM) methods, as well as observational and simulation methods, beginning with original diode and thyristor phase-controlled converters[6,7].

II. PROPOSED METHODOLOGY

By considering, NPC inverter as a test system based on single pole triple throw switch so that can be applied ±0.5V_{dc} and zero voltage at the load terminal is achieved (as shown in Fig. 1)

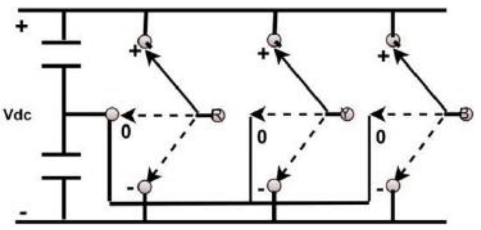

Fig.1. Multi-level inverter with single pole triple throw

As shown in Fig. 1, we have the option of either connecting it to the positive bus or DC midpoint or negative bus. Earlier, the DC midpoint in a two-level inverter is not available for making an electrical connection [7]. Sometimes load current may flow in or out of this particular point, and we have a single pole triple throw switch, so it is called a three-level inverter as shown in fig.2 .

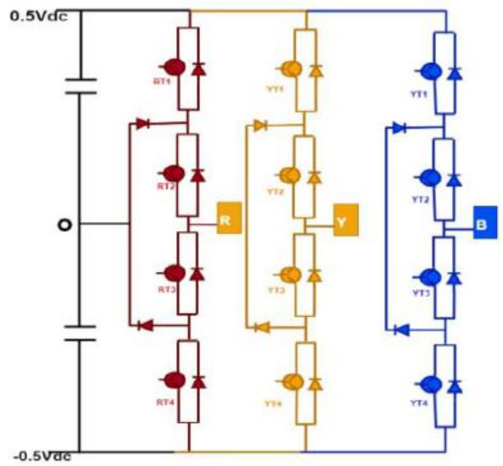

Fig.2. Multi-level neutral point clamped inverter

Various combinations of pole voltages are (using eqs. (1-2))

$$V_{RO} = 0, \pm \frac{V_{dc}}{2} \quad (1)$$

$$V_{YO} = 0, \pm \frac{V_{dc}}{2} \quad (2)$$

$$V_{BO} = 0, \pm \frac{V_{dc}}{2} \quad (3)$$

Similarly, the line-to-line voltage we can calculate by Eq. (1-3)

$$V_{RY} = V_{RO} - V_{YO} \quad (4)$$

$$V_{RY} = 0, \pm \frac{V_{dc}}{2}, \pm V_{dc} \quad (5)$$

The number of level counts on the basis of the line-to-line pole voltage so can also be called a 5-level inverter as we have shown by Eq. (5). Here, in this paper, the number of levels is equivalent to the number of pole voltages. The top two devices (T_1, T_2) are on the bottom two (T_3, T_4) off. In this case, R is connected to $\frac{V_{dc}}{2}$. Hence, this is the pole connected to the top throw. We can connect the pole to the bottom throw, by keeping T_1 ,T_2 off, andT_3 ,T_4 on. Therefore, we will have this pole connected to the bottom throw. Apparently, pole voltages can be 0, when the pole R is connected to O, by the middle two switches being on. The same way pole voltages of Y and B are zero if the middle two switches are on as shown in table 1.

Table1. Switching sequence with pole voltages

T_1	T_2	T_3	T_4	Pole Voltage
1	1	0	0	$0.5V_{DC}$
0	1	1	0	0
0	0	1	1	$0.5V_{DC}$

It is also possible to connect R to O; by turning off T_1, T_4 and onT_2,T_3. Therefore, R could establish a connection with O. Two different paths would depend on the load current. All switches have the bi-directional current flowing capability. Per phase load voltages is presenting by Eq. 6

$$V_{RN} = \frac{1}{3}(V_{RY} - V_{BR}) \quad (6)$$

Various combination of phase to neutral voltages as shown by Eq. 6

$$V_{RN} = 0, \pm \frac{V_{dc}}{3}, \pm \frac{V_{dc}}{2}, \pm \frac{V_{dc}}{6} \pm \frac{2V_{dc}}{3} \quad (7)$$

Hence, this converter can apply nine level of voltages at the pole regardless of the direction of the current and line to neutral voltages (as shown by Eq. 7). There are also two complementary switches pairs available T_1 , T_3 and T_2, T_4 i.e.in two-level inverter; there is one pair of complementary switches; now here two pairs of complementary switches.

III. RESULTS

Earlier, in STPWM for the two-level inverter, we could compare a one sine wave with one carrier wave [7]. Now in NPC for single sine wave with two carrier waves, because we have to produce two signals, it can also be with two sine waves with one carrier, but in our case, we consider one sine and two carrier waves.

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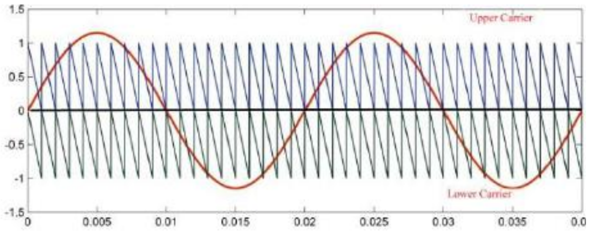

Fig.3. Carrier wave for NPC

There are two different carriers, one way of doing with the same R, Y, and B, but now there are two level-shifted carriers (as shown in Fig. 3). In Fig. 3, only the R phase is drawn; it is higher than both the carrier signals, then the R phase both the top switches on. If it is lower than the upper carrier wave but higher than the lower carrier wave, then the middle two switches are kept on. Similarly, it is lower than both the carrier waves the bottom two switches on.

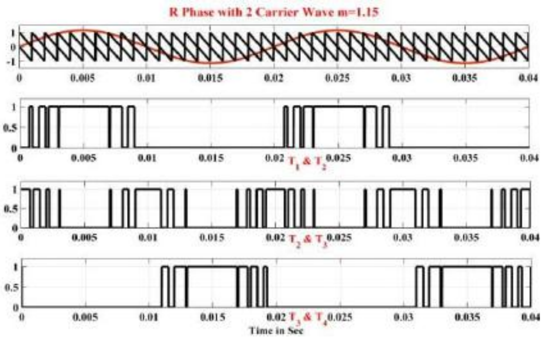

Fig.4. R phase with combined switching pairs (T_1 T_2, T_2 T_3, and T_3 T_4) at m=1.15.

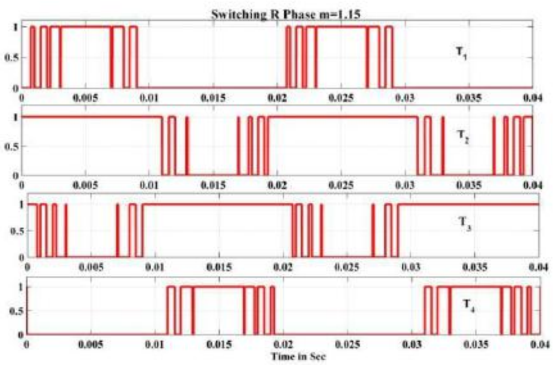

*Fig.**5.** R Phase has individual Switching Pairs (T_1, T_2, T_3 T_4) at m=1.15.*

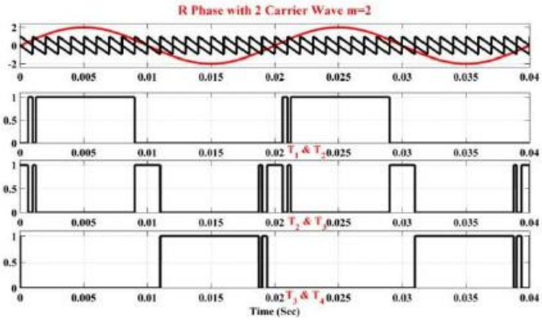

Fig.6. R Phase with Combined Switching Pairs (T_1 T_2, T_2 T_3, and T_3 T_4) at m=2.0

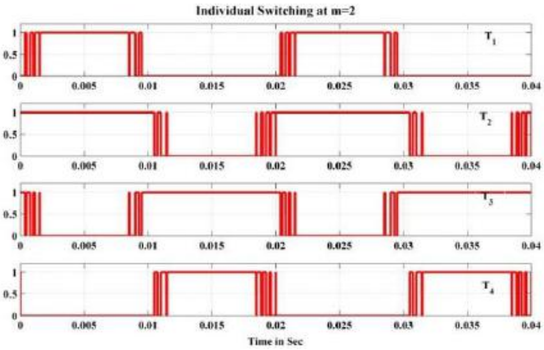

Fig.7. Switching Pulses for R Phase Switches at m=2.0

If we enter deeper modulation indexes (zone III) (as shown in figs. 4-7), in this case the switching operation is approximately equal to 6-step operation. It is valid for MLI also. In this case, the switching frequency is less; however, the THD is very high [7] in stand-alone PV systems.

IV. CONCLUSIONS

For a very high modulation indexes(m), then the switching operation is approximately equal to 6-step operation. It is valid for NPC-MLI also. In this case, the switching frequency is less; however, the THD is very high in stand-alone PV systems. In this case, low harmonic frequency voltage and current are very high, and to compensate for these ripples, we have to design the controller.

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